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## BURST COUNTER CONTROLLER AND METHOD IN A MEMORY DEVICE OPERABLE IN A 2-BIT PREFETCH MODE

### TECHNICAL FIELD

This invention relates to memory devices, and more particularly, to a  
5 burst counter controller and method for more efficiently generating column addresses  
when the memory device is operating in a burst access mode.

### BACKGROUND OF THE INVENTION

Memory devices, such as dynamic random access memories ("DRAMs")  
contain a large number of memory cells arranged in arrays having rows and columns. A  
10 memory cell is selected by a row address and a column address. The row address  
designates the row of the array containing the selected memory cell, and the column  
address designates the column of the array containing the selected memory cell. A  
series of memory cells can be selected by sequentially applying respective addresses to  
the memory device. However, it requires a significant period of time to decode and  
15 process each memory address, thereby slowing the rate at which the memory cells in the  
series can be selected. Furthermore, the need to generate a respective address to access  
each memory cell also slows the rate at which memory cells can be accessed and  
increases the processing overhead of circuitry interfacing with the memory device.

To avoid or at least alleviate the above-described problems, various  
20 modes have been devised to avoid the need to provide a row address and a column  
address for each memory access. For example, in a "page mode" access to a DRAM, a  
single row address is applied to the DRAM to select a row or "page" of memory cells.  
A sequence of column addresses is then applied to the DRAM to select a corresponding  
sequence of memory cells in respective columns in the selected row.

25 Although page mode memory accesses have the advantage of eliminating  
the need for a respective row address to access each of the memory cells except for the  
first memory cell, the time required to decode and process each column address  
nevertheless requires a significant amount of time. To eliminate the need to apply a

column address to the memory device to access each memory cell, "burst mode" memory devices have been developed. In a burst mode memory device, such as a burst mode DRAM, a starting row address and a starting column address are applied to the DRAM. The DRAM then activates the row of memory cells corresponding to the row address and internally generates a sequence of column addresses to access respective memory cells in the activated row. Burst access modes significantly increase the rate at which data may be read from or written to a memory device.

Sub B1  
Burst mode memory devices initially operated by serially accessing the memory cells in an active row. However, with the advent of synchronous DRAM ("SDRAMs") having two separately addressable arrays of memory cells, interleave memory accesses were introduced. In interleave memory accesses, the memory addresses increment by toggling the least significant bit ("LSB") every address, toggling the next to least significant bit ("NLSB") every other address, toggling the next most significant bit every fourth address, etc. To further increase memory access speeds, a 2-bit prefetch mode of operation was developed. In the 2-bit prefetch mode of operation, the LSB of an address is ignored, and corresponding columns in respective arrays are thus simultaneously accessed using the address designated by all but the LSB of the column address. The column that is accessed in each array is thus designated by the NLS and higher bits NLSB and, as a practical matter, should be the same for both arrays so that corresponding columns in both arrays are simultaneously accessed.

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As explained in greater detail below, the burst mode addressing sequence for a memory device is different in the interleave mode than it is in the serial mode. Furthermore, the difficulties of accommodating both the serial mode and the interleave mode are exacerbated by operation in the 2-bit prefetch mode. In the 2-bit prefetch mode, a memory cell in an odd memory array (normally designated by an odd address) and a memory cell in an even memory array (normally designated by an even address) should be simultaneously accessed. In such cases, as previously explained, the least significant bit ("LSB") of a starting memory address is ignored because the LSB normally designates either an even memory array or an odd memory array.

Sub  
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The sequence of column addresses that should be generated starting at an initial, externally applied column address of "CA<sub>N</sub>...CA<sub>2</sub>, CA<sub>1</sub>, CA<sub>0</sub>" (where "CA<sub>0</sub>" is the LSB, "CA<sub>1</sub>" is the NLSB, and "CA<sub>N</sub>...CA<sub>2</sub>" are higher order bits) are shown below (ignoring the bits that are higher order than CA<sub>3</sub>). The address sequence for an 5 interleave mode with a starting column address of "0 1 1 0" is as follows:

BECAUSE  
NLSB = 0  
↓  
BETTER  
EXAMPLE

10

"0 1 1 0" (starting column address)

~~"0 1 1 1"~~

~~"1 0 0 0"~~

~~"1 0 0 1"~~

~~"1 0 1 0"~~

~~"1 0 1 1"~~

~~"1 1 0 0"~~

~~"1 1 0 1"~~

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CORRECT

0	1	1	0
0	1	1	1
0	1	0	0
0	1	0	1
0	0	1	0
0	0	1	1
0	0	0	0
0	0	0	1

1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1

Sub  
B3

The address sequence for an interleave mode with a starting column address of "0 1 0 1" is as follows:

20

"0 1 0 1" (starting column address)

~~"0 1 0 0"~~

~~"0 1 1 1"~~

~~"0 1 1 0"~~

~~"1 0 0 1"~~

~~"1 0 0 0"~~

~~"1 0 1 1"~~

~~"1 0 1 0"~~

D.P. 03/19/01  
S.S. 03/20/01

0	1	0	1
0	1	0	0
0	1	1	1
0	1	1	0
0	0	0	1
0	0	0	0
0	0	1	1
0	0	1	0

Sub  
B4

The address sequence for a serial mode with a starting column address of "0 1 1 0" is as follows:

30

"0 1 1 0" (starting column address)

~~"0 1 1 1"~~

~~"1 0 0 0"~~

~~"1 0 0 1"~~

~~"1 0 1 0"~~

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0	1	1	0
0	1	1	1
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1

~~"0 1 1"~~  
~~"1 1 0 0"~~  
~~"1 1 0 1"~~

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A<sub>5</sub>

In all cases, the LSB in all of the above examples is ignored by the memory devices, as previously explained. In each of the above examples, the ~~NLSB~~ selects the same column in each pair of addresses, and the LSB, which is ignored in the SDRAM, is effectively "0" for the even array and "1" for the odd array. For example, the first pair of column addresses in the interleaved mode with a starting column address of "0 1 1 0" selects a column in both arrays having a NLSB (i.e., an effective LSB) of "1", and the second pair of column addresses selects a column in both arrays having a NLSB (i.e., an effective LSB) of "0."

NLS AND  
HIGHER BITS  
SELECT

USED FOR  
OTHER  
PURPOSES  
THAT COLUMN

Sub  
B<sub>6</sub>

In all of the above cases, the sequence of column addresses can be generated by an incrementing a burst counter that generates only the NLSB and all bits more significant than the NLSB since the LSB is ignored by a memory device and the counter. Note, however, a problem that develops in the serial mode where the starting column address is "0 1 0 1":

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"0 1 0 1" (starting column address)  
"0 1 1 0"  
"0 1 1 1"  
"1 0 0 0"  
"1 0 0 1"  
"1 0 1 0"  
"1 0 1 1"  
"1 1 0 0"

In this case, the NLSB selects a different column in each pair of column addresses. For example, the "0" NLSB bit of the first column address in the first pair of addresses selects a column in one array designated by an address ending in "0" and the "1" NLSB bit of the second column address in the first pair of addresses selects a column in the other array designated by an address ending in "1." Similarly, the "1" NLSB bit of the first column address in the second pair of addresses selects a column in

one array designated by an address ending in "1" and the "0" NLSB bit of the second column address in the second pair of addresses selects a column in the other array designated by an address ending in "0." As a result, the two bits of accessed data are stored in different columns of the arrays, thus making it difficult to subsequently access the same two bits of data.

Similarly, in the interleave mode with a starting column address of "0 0 1 1" the address sequence must be as follows:

"0 0 1 1" (starting column address)

"0 0 1 0"

10

"0 0 0 1"

"0 0 0 0"

"0 1 1 1"

"0 1 1 0"

"0 1 0 1"

"0 1 0 0"

15  
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a serial increment of

The above address sequence cannot be generated by incrementing a burst counter since the addresses in the above sequence (again, ignoring the LSB) do not increment. Thus, an interleave sequence for certain starting addresses cannot be generated in the 2-bit prefetch mode by simply incrementing a burst counter.

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burst

Conventional burst mode 2-bit prefetch memory devices capable of operating in either a serial mode or an interleave mode generally require two different burst mode counters, one of which is used in the serial mode and the other of which is used in the interleave mode. The need for separate burst accessing circuitry for each of these two burst modes significantly increases the cost of memory devices operating in these two modes.

25

There is therefore a need for a burst mode column addressing circuit and method for a 2-bit prefetch memory device that can operate in both a serial mode and an interleave mode thereby eliminating the need for separate addressing and counting circuitry for each mode.

## SUMMARY OF THE INVENTION

A burst counter method and circuit is used for addressing a memory device capable of operating in 2-bit prefetch mode in either or both of a serial mode and an interleave mode. A column address counter generates all but the least significant bit ("LSB") of a series of column addresses starting at an externally applied initial address. In the interleave mode, a counter control circuit causes the column address counter to increment responsive to decoding a logic "0" value for the next to least significant bit ("NLSB") of the initial column address, and to decrement responsive to decoding a logic "1" value for the NLSB of the initial column address. In the serial mode, the counter control circuit causes the column address counter to increment responsive to decoding a logic "0" value for the LSB of the initial column address, and to decrement responsive to decoding a logic "1" value for the LSB of the initial column address.

## BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram of a memory device including a burst mode counter according to one embodiment of the invention.

Figure 2 is a block diagram of a portion of a burst mode counter usable in the memory device of Figure 1 according to one embodiment of the invention.

Figure 3 is a logic diagram of one embodiment of a counter control device used in the burst mode counter portion shown in Figure 2.

Figure 4 is a block diagram of a computer system using the memory device of Figure 1 containing an embodiment of a burst mode counter in accordance with the invention.

## DETAILED DESCRIPTION OF THE INVENTION

A memory device that may use a burst mode counter according to one embodiment of the invention is shown in Figure 1. The memory device illustrated therein is a synchronous dynamic random access memory ("SDRAM") 10, although the invention can be embodied in other types of DRAMs, such as packetized DRAMs and RAMBUS DRAMs (RDRAMs), as well as other types of memory devices, such as

static random access memories ("SRAMs"). The SDRAM 10 includes an address register 12 that receives either a row address or a column address on an address bus 14. The address bus 14 is generally coupled to a memory controller (not shown in Figure 1). Typically, a row address is initially received by the address register 12 and applied to a row address multiplexer 18. The row address multiplexer 18 couples the row address to a number of components associated with either of two memory banks 20, 22 depending upon the state of a bank address bit forming part of the row address. Associated with each of the memory banks 20, 22 is a respective row address latch 26 which stores the row address, and a row decoder 28 which applies various signals to its respective array 20 or 22 as a function of the stored row address. The row address multiplexer 18 also couples row addresses to the row address latches 26 for the purpose of refreshing the memory cells in the arrays 20, 22. The row addresses are generated for refresh purposes by a refresh counter 30, which is controlled by a refresh controller 32.

After the row address has been applied to the address register 12 and stored in one of the row address latches 26, a column address is applied to the address register 12. The address register 12 couples the column address to a column address latch 40. Depending on the operating mode of the SDRAM 10, the column address is used for either of two purposes. First, in a normal operating mode, the column address is coupled through a burst counter 42 to a column address buffer 44 to select a column of memory cells in one or both of the memory arrays 20, 22. Second, in a burst operating mode, the column address is coupled to the burst counter 42 and used as a starting column address ("SCA"). The burst counter then generates a sequence of column addresses starting at the SCA, and applies the sequence of column addresses to the column address buffer 44. In either case, the column address buffer 44 applies a column address to a column decoder 48a,b for each array 20, 22. The column decoders 48a,b apply respective decoded column addresses to respective sense amplifiers and associated column circuitry 50, 52 for the respective arrays 20, 22.

Data to be read from one of the arrays 20, 22 is coupled to the column circuitry 50, 52 for one of the arrays 20, 22, respectively. The data is then coupled through a read data path 54 to a data output register 56, which applies the data to a data



bus 58. Data to be written to one of the arrays 20, 22 is coupled from the data bus 58 through a data input register 60 and a write data path 62 to the column circuitry 50, 52 where it is transferred to one of the arrays 20, 22, respectively. A mask register 64 may be used to selectively alter the flow of data into and out of the column circuitry 50, 52, such as by selectively masking data to be read from the arrays 20, 22.

The above-described operation of the SDRAM 10 is controlled by a command decoder 68 responsive to command signals received on a control bus 70. These high level command signals, which are typically generated by a memory controller (not shown in Figure 1), are a clock enable signal CKE\*, a clock signal CLK, a chip select signal CS\*, a write enable signal WE\*, a row address strobe signal RAS\*, and a column address strobe signal CAS\*, which the "\*" designating the signal as active low. Various combinations of these signals are registered as respective commands, such as a read command or a write command. The command decoder 68 generates a sequence of control signals responsive to the command signals to carry out the function (e.g., a read or a write) designated by each of the command signals. These command signals, and the manner in which they accomplish their respective functions, are conventional. Therefore, in the interest of brevity, a further explanation of these control signals will be omitted.

The read data path 54 from the column circuitry 50, 52 to the data output register 56 includes one or more pairs of complimentary input/output ("I/O") lines (not shown in Figure 1) that couple data from a sense amplifier (not shown) for each column in each array 20, 22, respectively. The sense amplifier in the column circuitry 50, 52 for an addressed column receives complimentary signals from a pair of complimentary digit lines. The digit lines are, in turn, coupled to a pair of the complimentary I/O lines by column addressing circuitry. Each pair of I/O lines is selectively coupled by a pair of complimentary data lines to the complimentary inputs of a DC sense amplifier (not shown) included in the read data path 54. The DC sense amplifier, in turn, outputs data to the data output register 56, which is coupled to output or "DQ" terminals of the memory device 10.

One embodiment of a portion of the burst counter 42, which is shown in Figure 2, includes a column address counter 100 and counter control circuit 104. The column address counter 100 and the counter control circuit 104 are shown in Figure 2 along with the column address buffer 44, column address decoders 48a,b, and memory arrays 20, 22 used in the SDRAM 10 of Figure 1. The operation of the burst counter 42 is based on the realization that the correct sequence of column addresses can be generated in the 2-bit prefetch serial mode by decrementing the column address counter whenever the LSB of the externally applied starting column address SCA<0> is a "1." The operation of the burst counter 42 is further based on the realization that the correct sequence of column addresses can be generated in the 2-bit prefetch interleave mode by decrementing the column address counter whenever the NLSB of the externally applied starting column address SCA<1> is a "1."

For example, in the serial mode using the above example of a starting column address of "0 1 0 1" the correct sequence is:

15 "1 1 0 1" (starting column address)  
 "1 1 0 0"  
 "1 0 1 1"  
 "1 0 1 0"  
 "1 0 0 1"  
 20 "1 0 0 0"  
 "1 1 1 1"  
 "1 1 1 0"

*Sub Bio*  
*10.03/24/01*  
*S.S. 3/20/01*

Again, ignoring the LSB, it can be seen that the above sequence consists of a decrementing count, and that the column address for each pair of addresses is the same for both the even and the odd addresses in each pair.

In the interleave mode, the correct sequence of column addresses for a starting column address of "1 0 1 1" is as follows:

30 "1 0 1 1"  
 "1 0 1 0"  
 "1 0 0 1"

*Sub BII*

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1	0	0	0
1	1	1	1
0	1	1	0
0	1	0	1
0	1	0	0

5

Again ignoring the LSB, it can be seen that the above sequence consists of a decrementing count in which the bits toggle correctly for an interleave sequence as explained above, and that the column address for each pair of addresses is the same for both the even and the odd addresses in each pair.

10

Returning, now, to Figure 2, the bust counter 42 implements the above principle of operation by controlling the count direction of the column address counter 100 using the counter control circuit 104 based on an INTL signal and the two least significant bits  $SCA<0:1>$  of the externally applied starting column address  $SCA<N:0>$ . The INTL signal is active high in the interleave mode and inactive low in the serial mode. The column address counter 100 receives  $SCA<N:1>$ , i.e., all but the LSB of the starting column address  $SCA<N:0>$ , from the column address latch 40 (Figure 1) or other circuit. The counter circuit 100 generates a sequence of multi-bit column addresses  $CA<N:1>$  responsive to a clock signal CLK. The first of these multi-bit column addresses  $CA<N:1>$  consists of all but the LSB of the starting column address  $SCA<N:0>$  that was initially applied to the counter 100. Thus, the LSB of the column addresses  $CA<N:1>$  corresponds to the NLSB of the starting column address  $SCA<N:0>$ .

As previously mentioned, the count direction of the column address counter 100 is controlled by the counter control circuit 104. The counter control circuit 104 generates a DEC signal that is active high to cause the counter control circuit 104 to decrement responsive to the CLK signal whenever the LSB of the starting address, i.e.,  $SCA<0>$ , is "1" when operating in the serial mode. The counter control circuit 104 also generates a logic "1" DEC signal whenever the NLSB of the starting address, i.e.,  $SCA<1>$ , is "1" when operating in the interleave mode. In all other cases, the counter

25

control circuit 104 generates a logic "0" DEC signal, which causes the column address counter 100 to increment.

By using a single counter that can either increment or decrement, and by controlling the count direction of the counter responsive to the state of the LSB in the serial mode and responsive to the state of the NLSB in the interleave mode, the  
 5 embodiments of the invention are able to generate the proper column address sequences without the need for separate address sequence generators for the serial and interleave modes.

One embodiment of the counter control circuit 104 is shown in Figure 3.

10 The counter control circuit 104 generates an active "1" DEC signal at the output of a NOR gate 120 whenever either of the inputs to the NOR gate 120 is low. The first input to the NOR gate 120 will be low whenever a NOR gate 124 decodes a high LSB of the starting column address  $SCA<0>$  and a high output from an inverter 126, which occurs whenever INTL is low indicative of operation in the serial mode. The second input to  
 15 the NOR gate 120 will be low whenever another NOR gate 128 decodes a high NLSB of the starting column address  $SCA<1>$  and an active high INTL signal indicative of operation in the interleave mode. Thus, the NAND gate 120 will generate an active high DEC signal whenever the LSB of the starting column address is "1" when operating in the serial mode or whenever the NLSB of the starting column address is  
 20 "1" when operating in the interleave mode.

The portion of the burst counter 42 shown in Figure 2 and 3 can be used in the SDRAM 10 shown in Figure 1, and the resulting SDRAM 10 can be used in a computer system, such as a computer system shown in Figure 4. The computer system  
 300 includes a processor 302 for performing various computing functions, such as  
 25 executing specific software to perform specific calculations or tasks. The processor 302 includes a processor bus 304 that normally includes an address bus, a control bus, and a data bus. In addition, the computer system 300 includes one or more input devices 314, such as a keyboard or a mouse, coupled to the processor 302 to allow an operator to interface with the computer system 300. Typically, the computer system 300 also  
 30 includes one or more output devices 316 coupled to the processor 302, such output

devices typically being a printer or a video terminal. One or more data storage devices 318 are also typically coupled to the processor 302 to allow the processor 302 to store data in or retrieve data from internal or external storage media (not shown). Examples of typical storage devices 318 include hard and floppy disks, tape cassettes, and compact disk read-only memories (CD-ROMs). The processor 302 is also typically coupled to cache memory 326, which is usually static random access memory ("SRAM"), and to the SDRAM 10 through a memory controller 330. The memory controller 330 normally includes a control bus 336 and an address bus 338 that are coupled to the SDRAM 10. A data bus 340 is coupled from the SDRAM 10 to the processor bus 304 either directly (as shown), through the memory controller 330, or by some other means.

From the foregoing it will be appreciated that, although specific embodiments of the invention have been described herein for purposes of illustration, various modifications may be made without deviating from the spirit and scope of the invention. For example, although the burst counter in accordance with the invention has been explained in the context of an SDRAM 10 having 2 memory arrays 20, 22 and a 2-bit prefetch, it will be understood that other embodiments of the invention may be used with memory devices having a greater number of memory arrays and/or operating to prefetch a number of bits greater than two. Other variations will also be apparent to one skilled in the art. Accordingly, the invention is not limited except as by the appended claims.